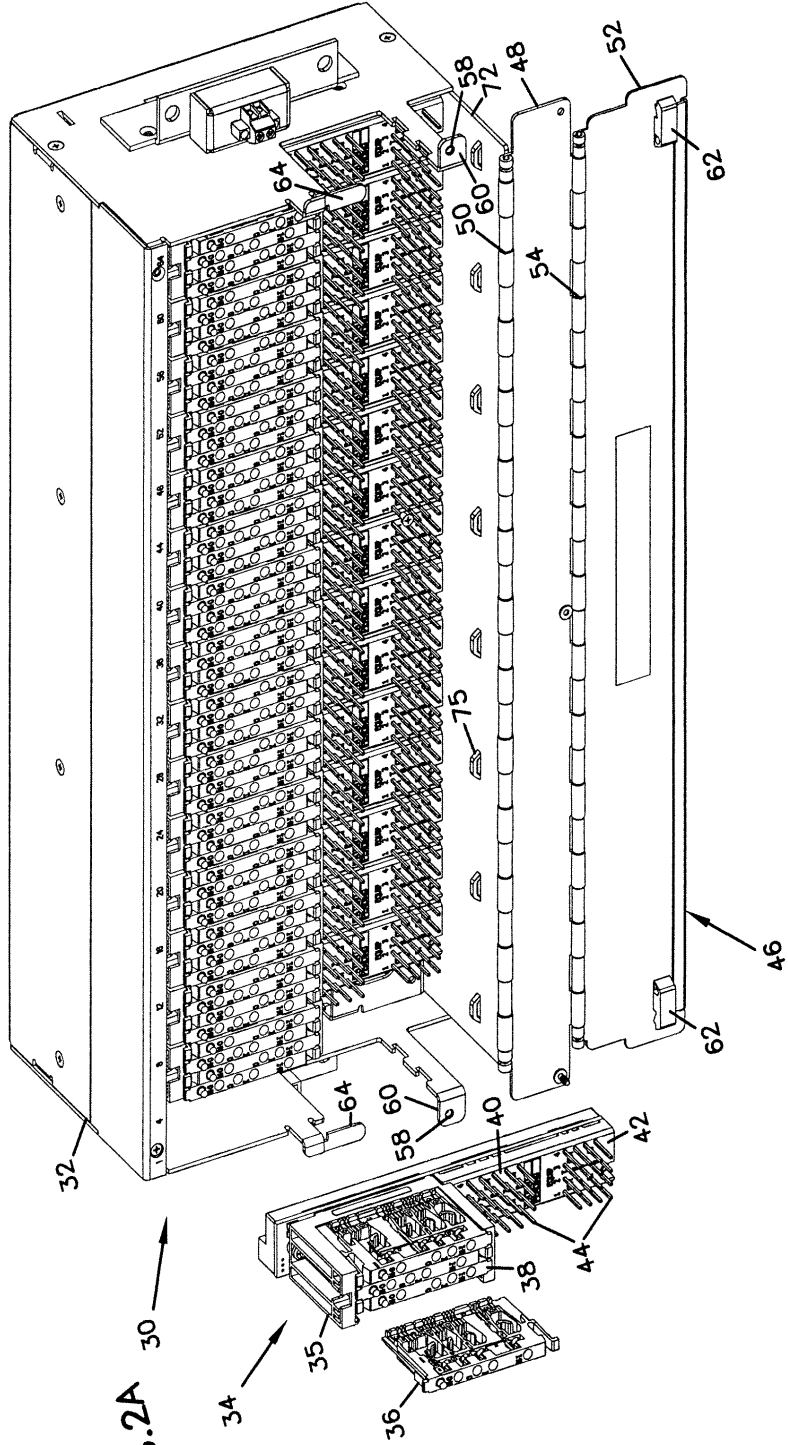


FIG. 1  
PRIOR ART

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**FIG. 2A**



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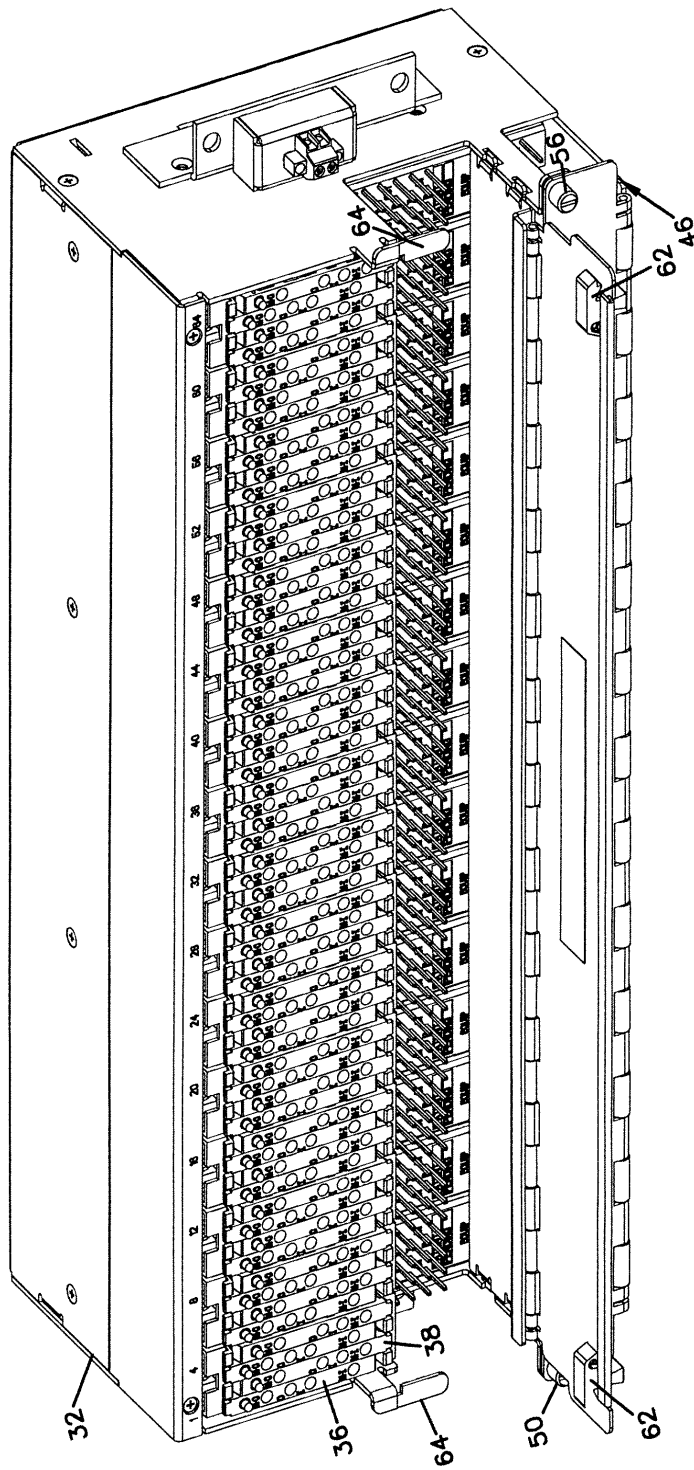


FIG. 2B

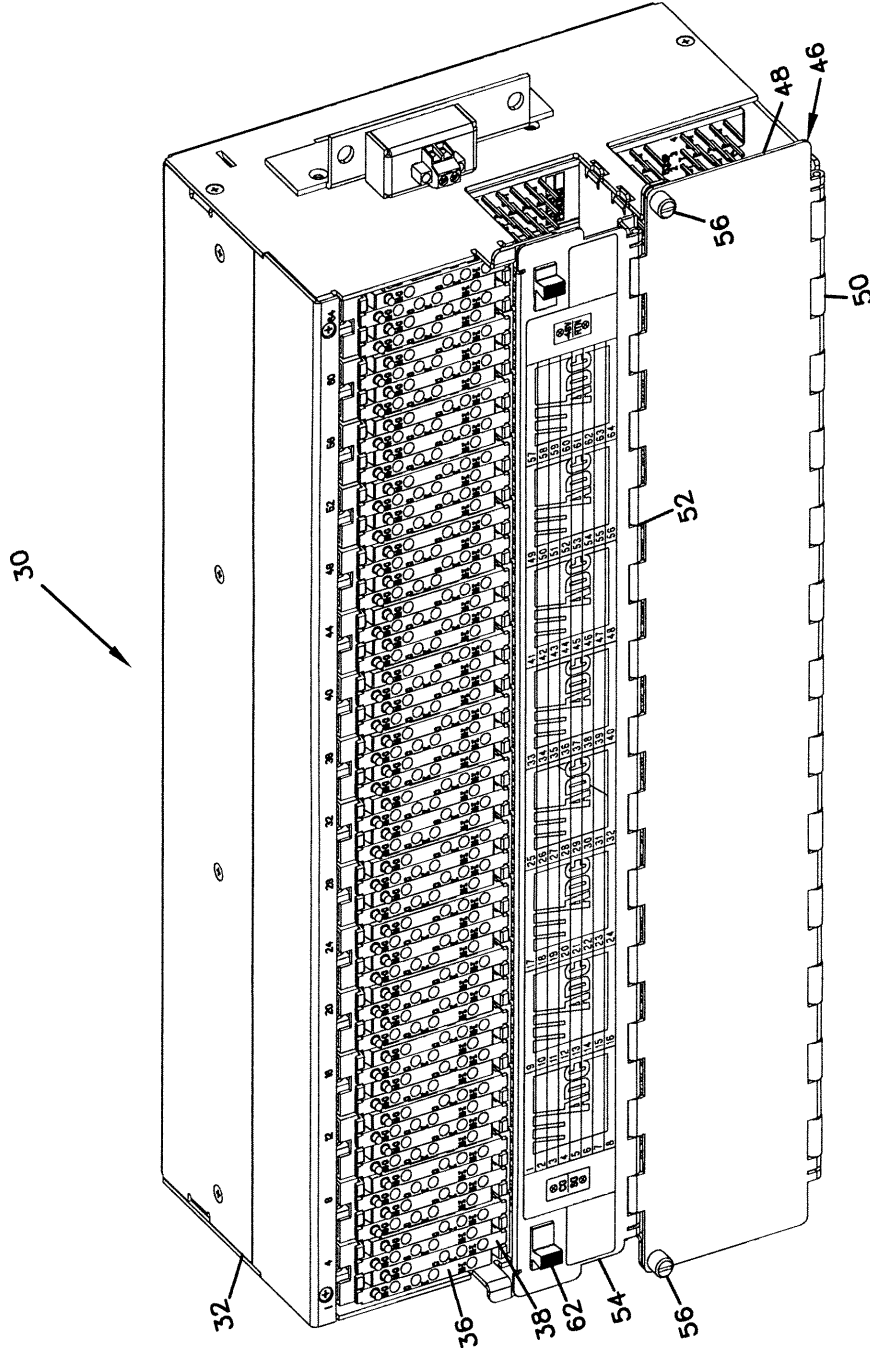


FIG. 2C

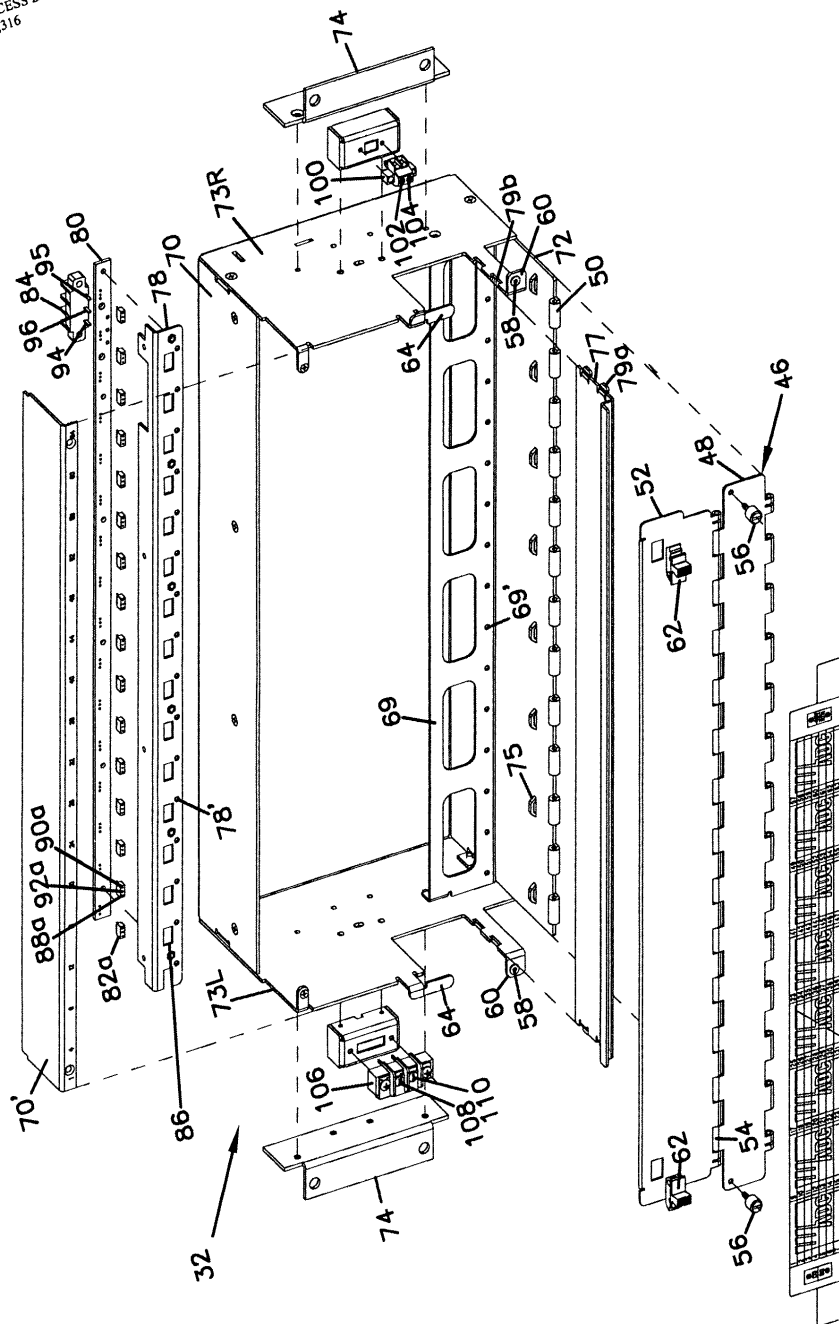


FIG. 3

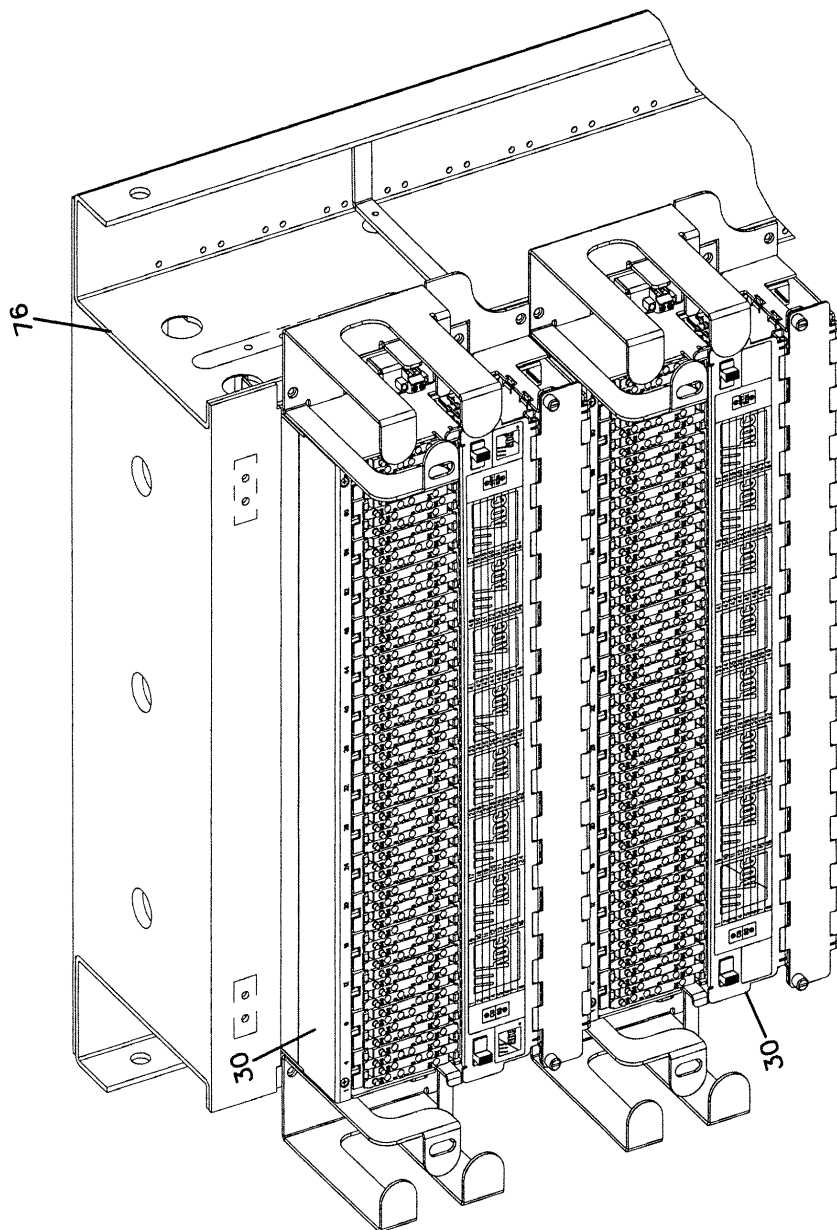


FIG. 4



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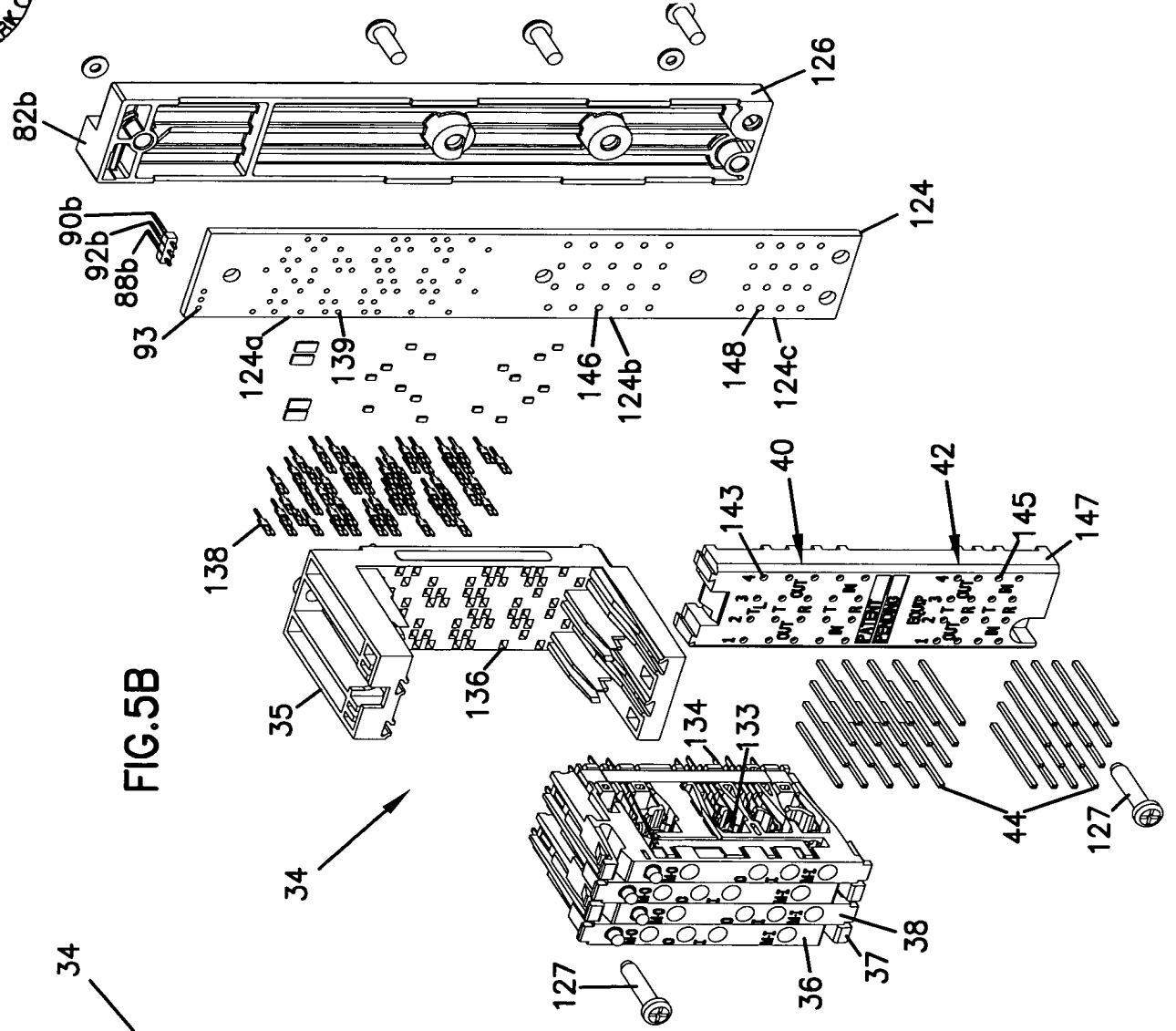


FIG. 5B

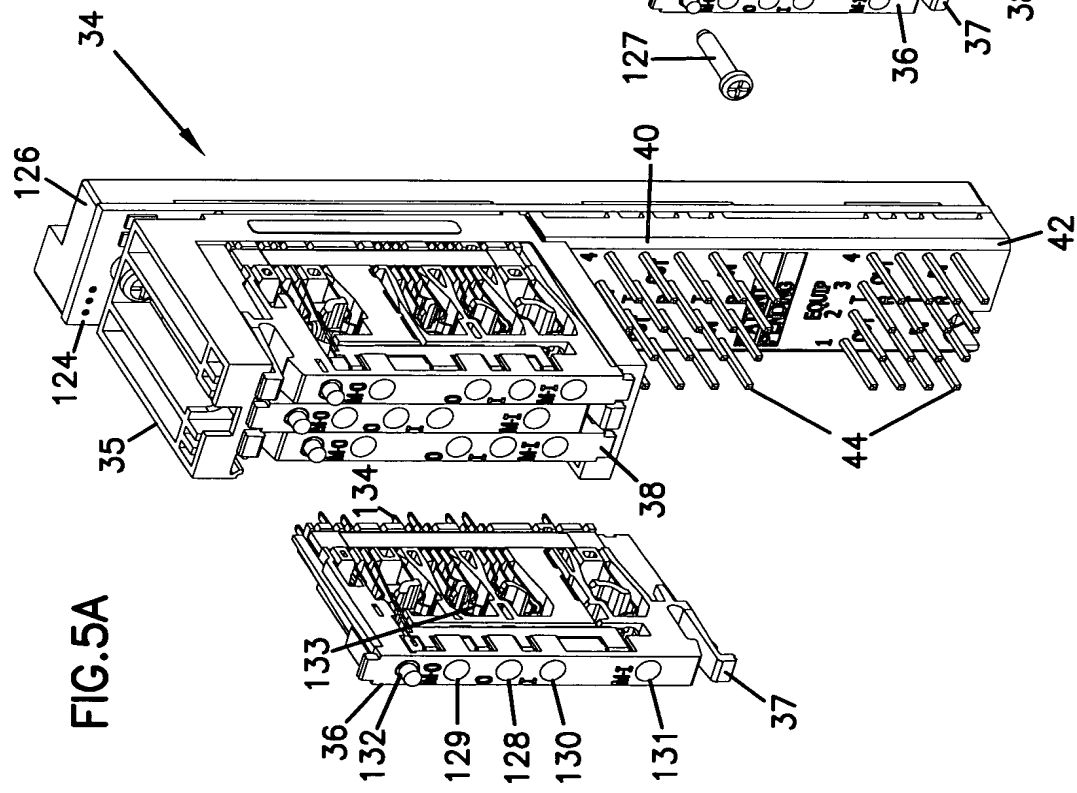
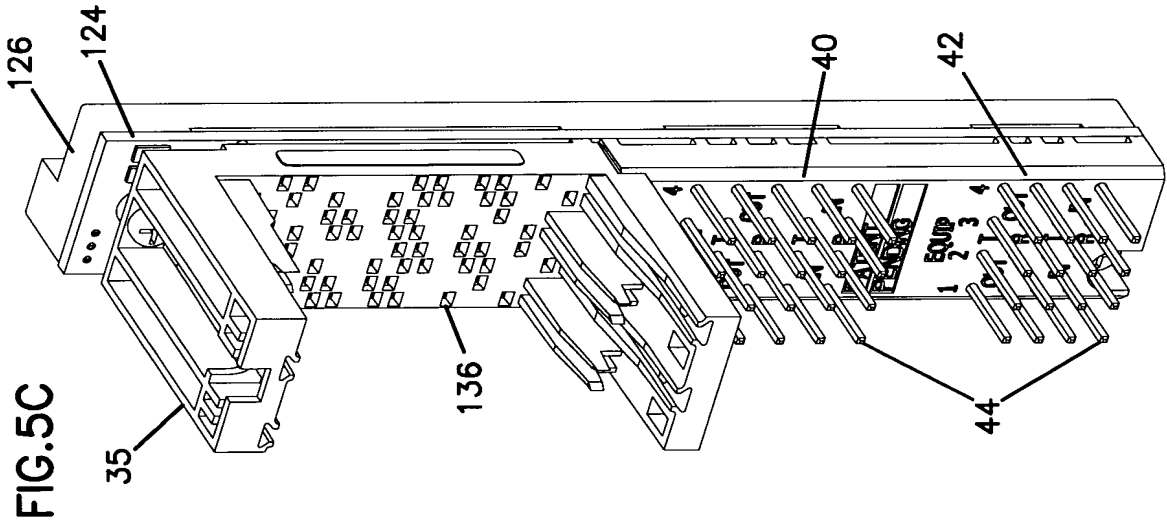
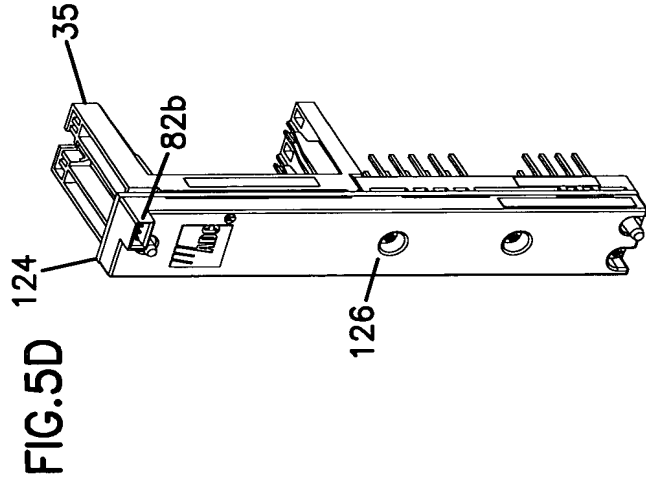


FIG. 5A







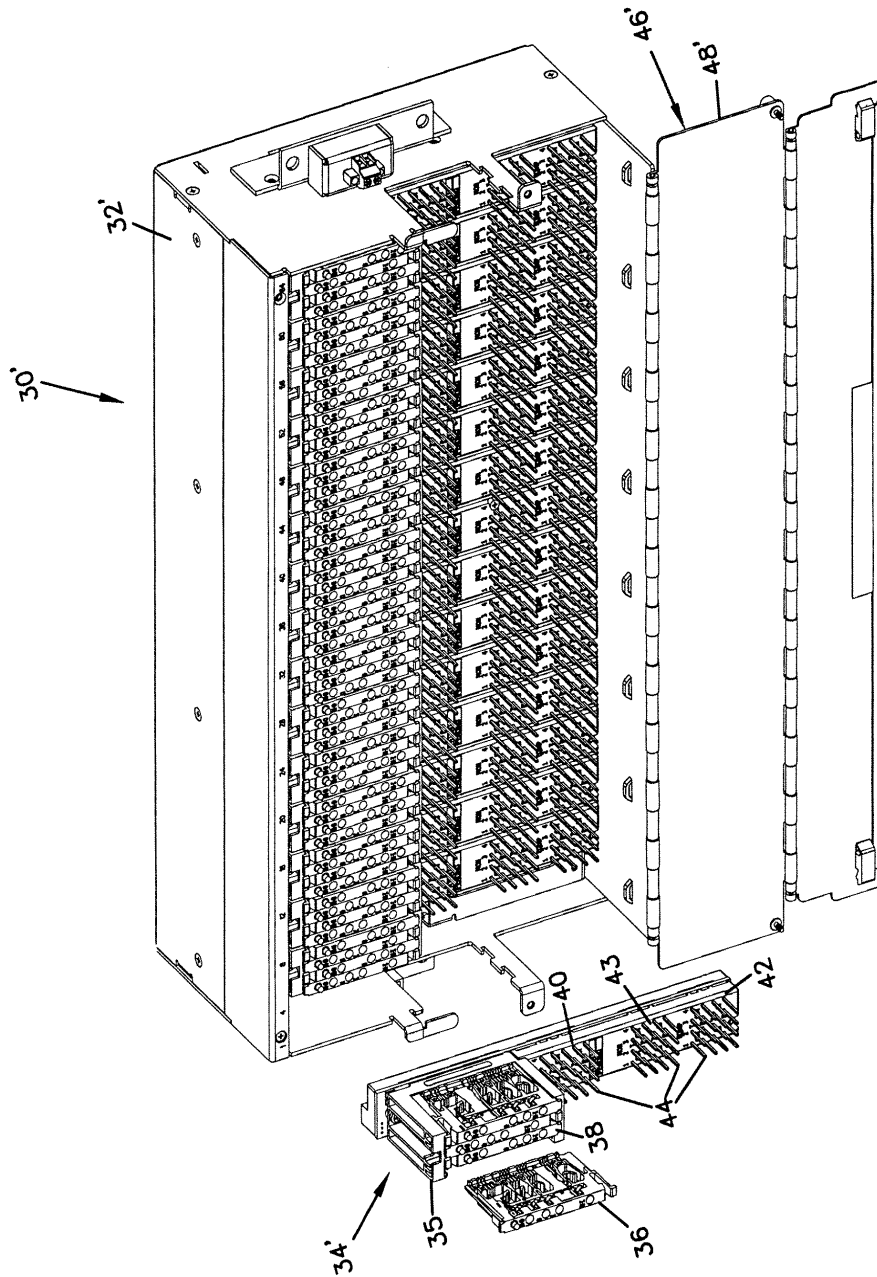


FIG. 7A



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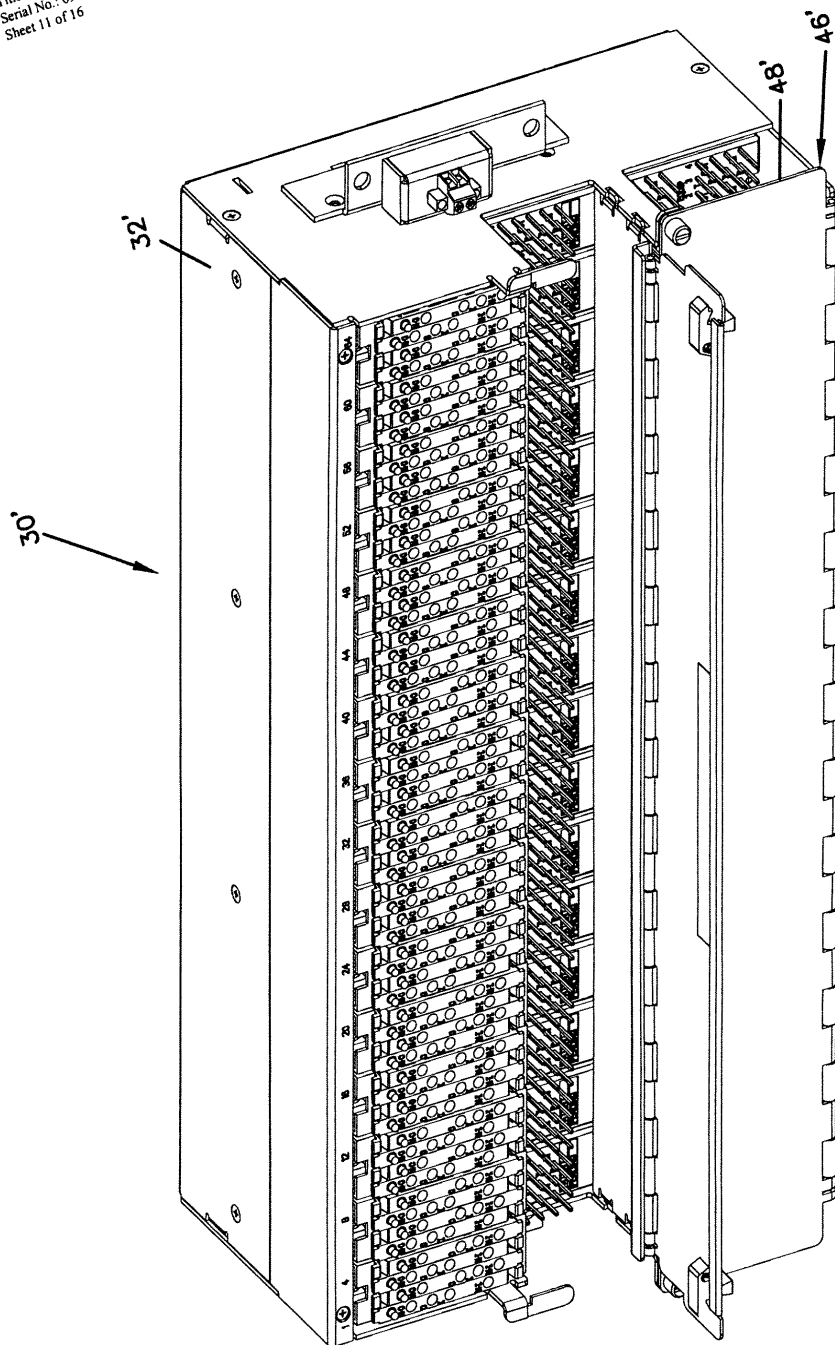


FIG. 7B



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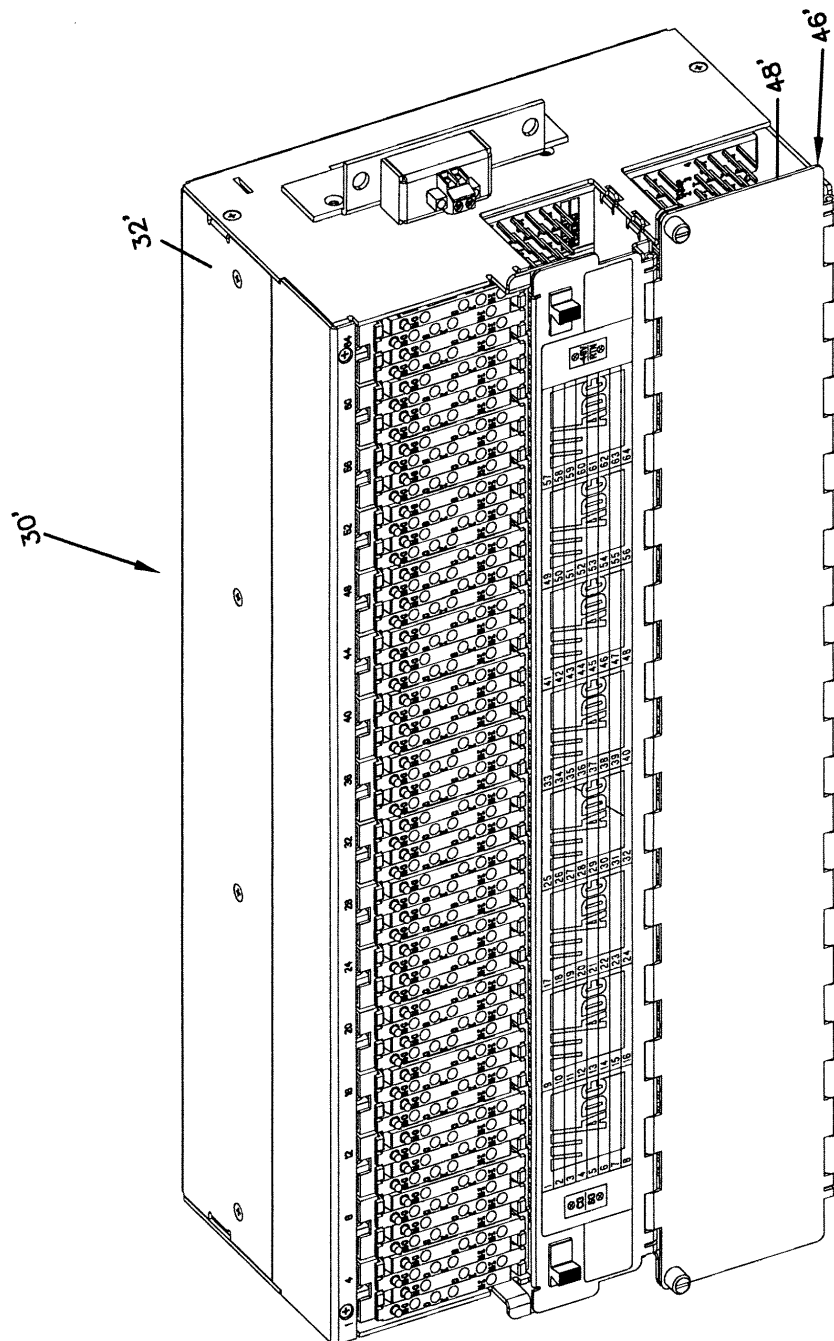


FIG. 7C



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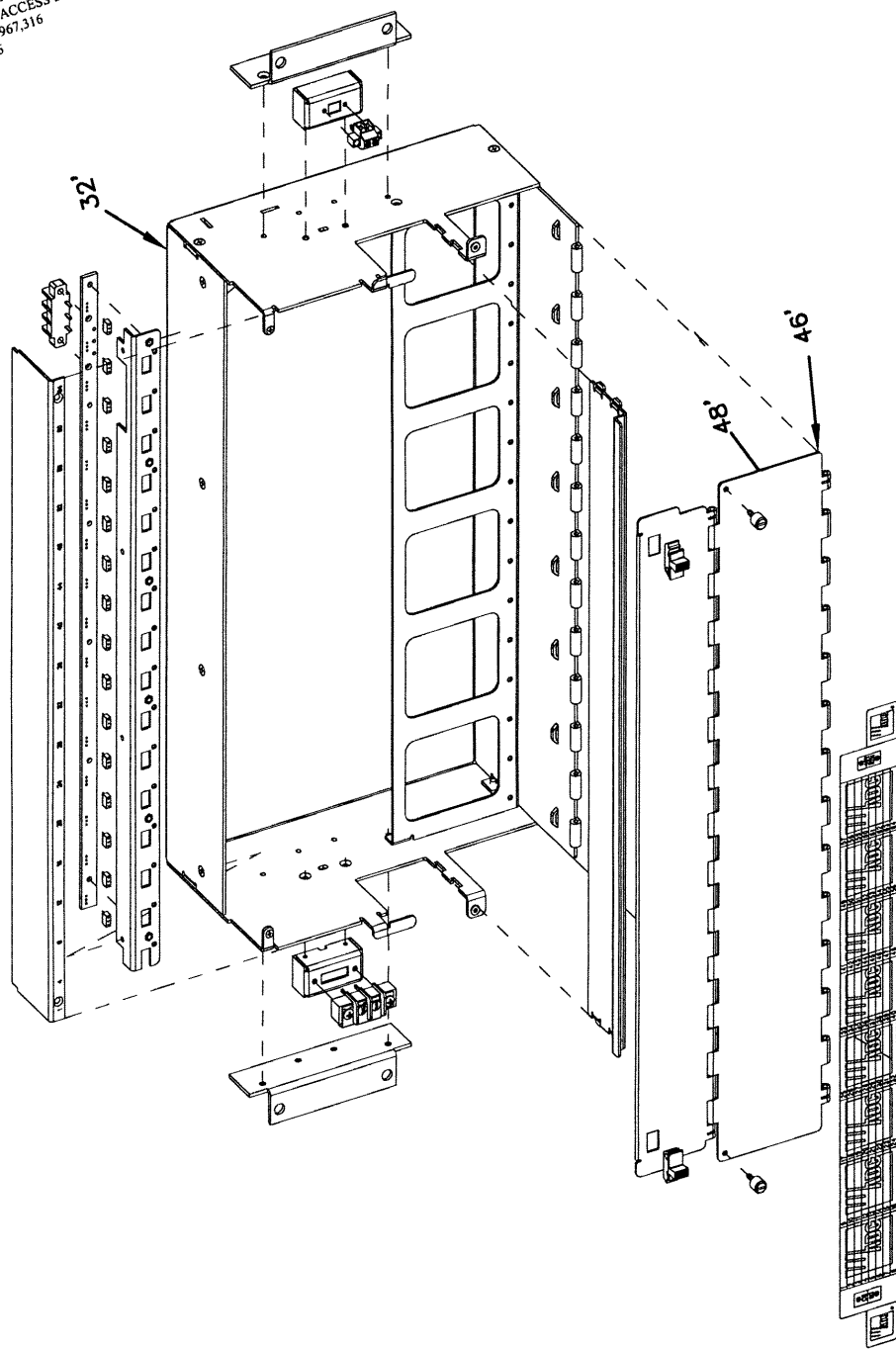
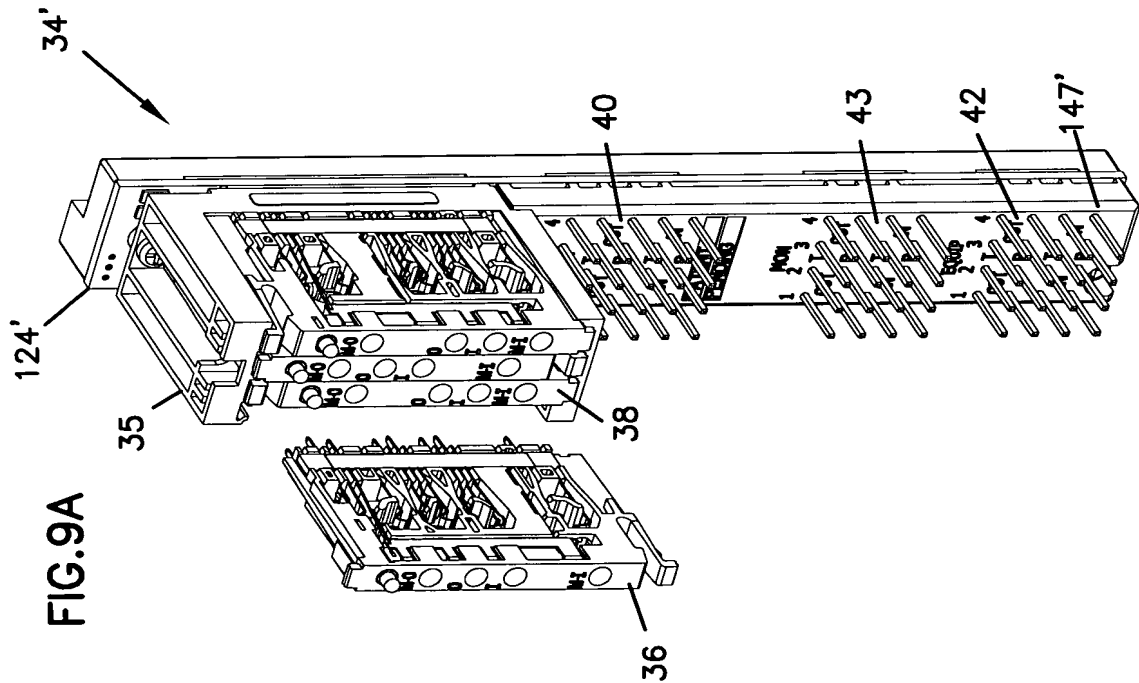
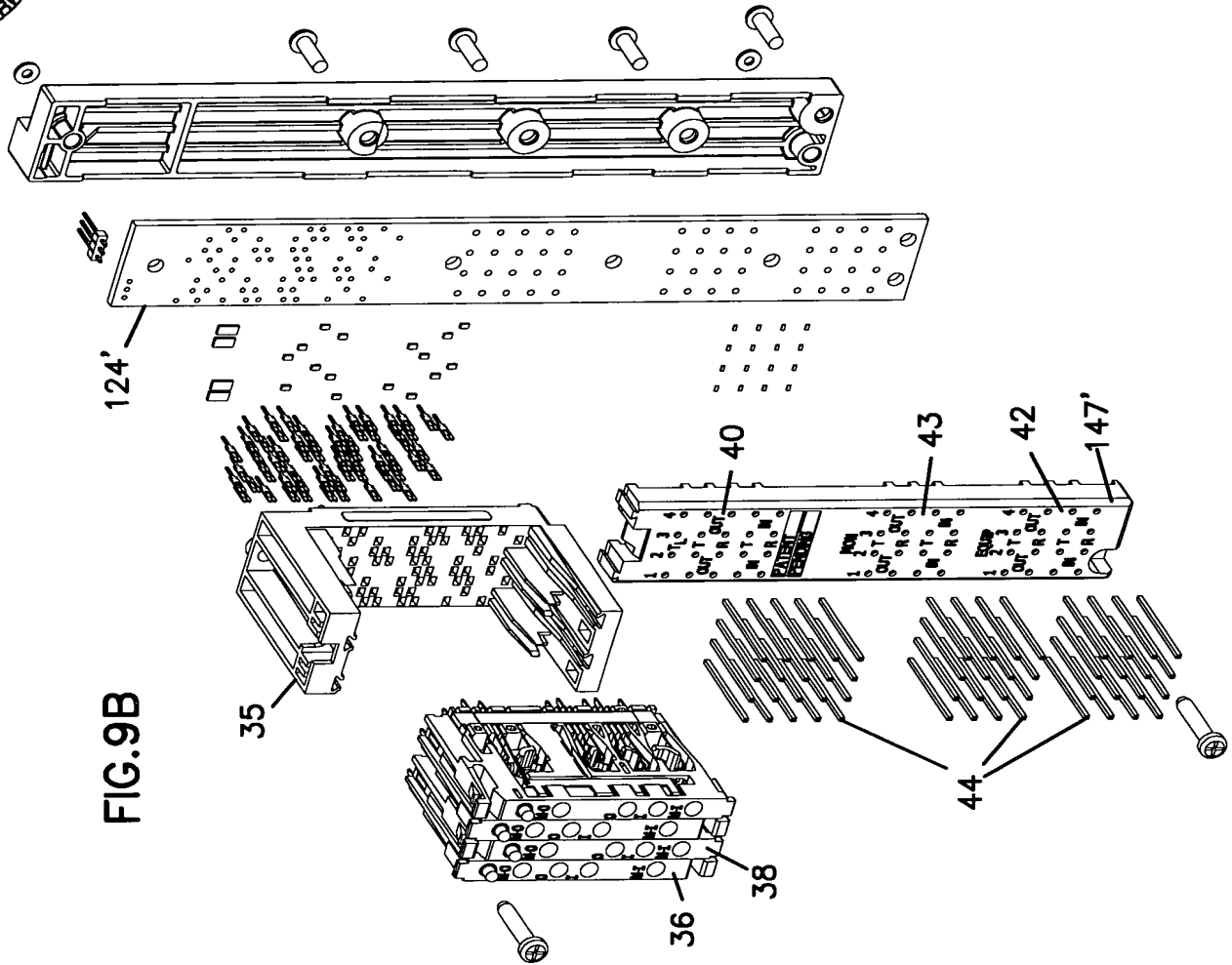


FIG. 8



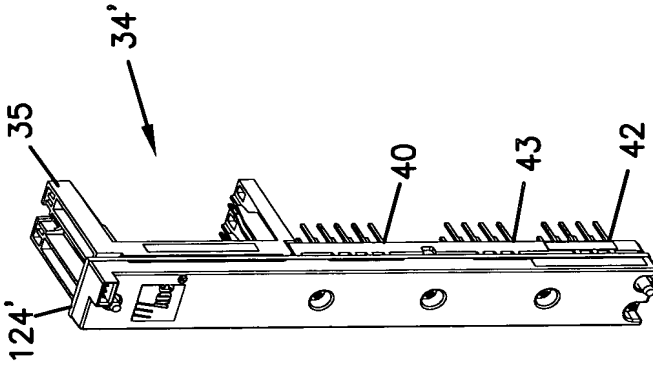


FIG. 9D

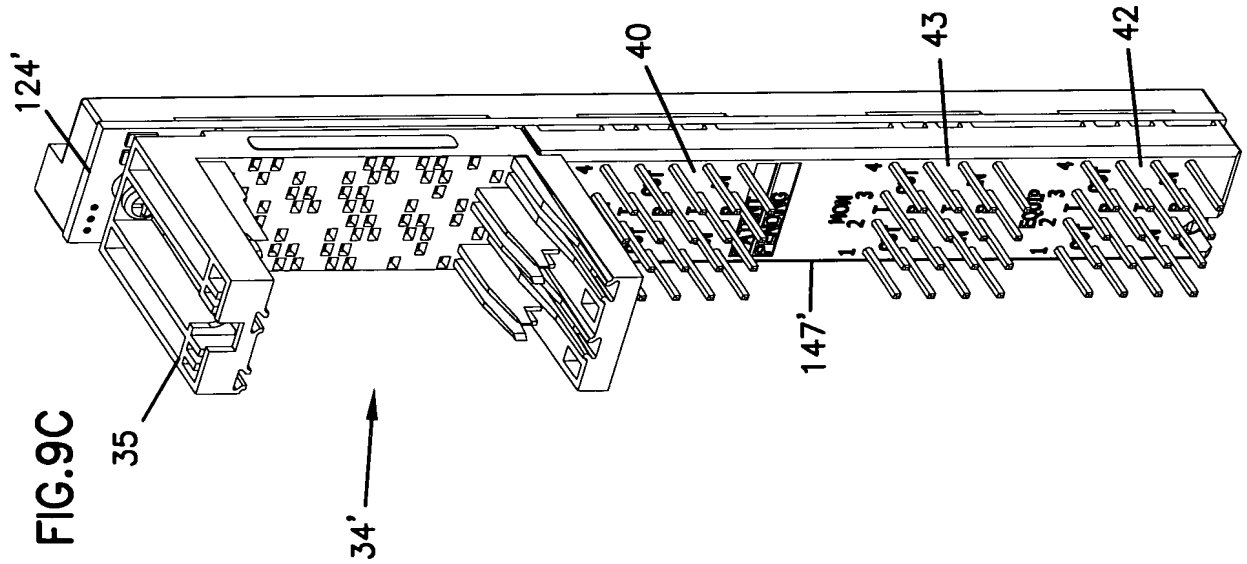
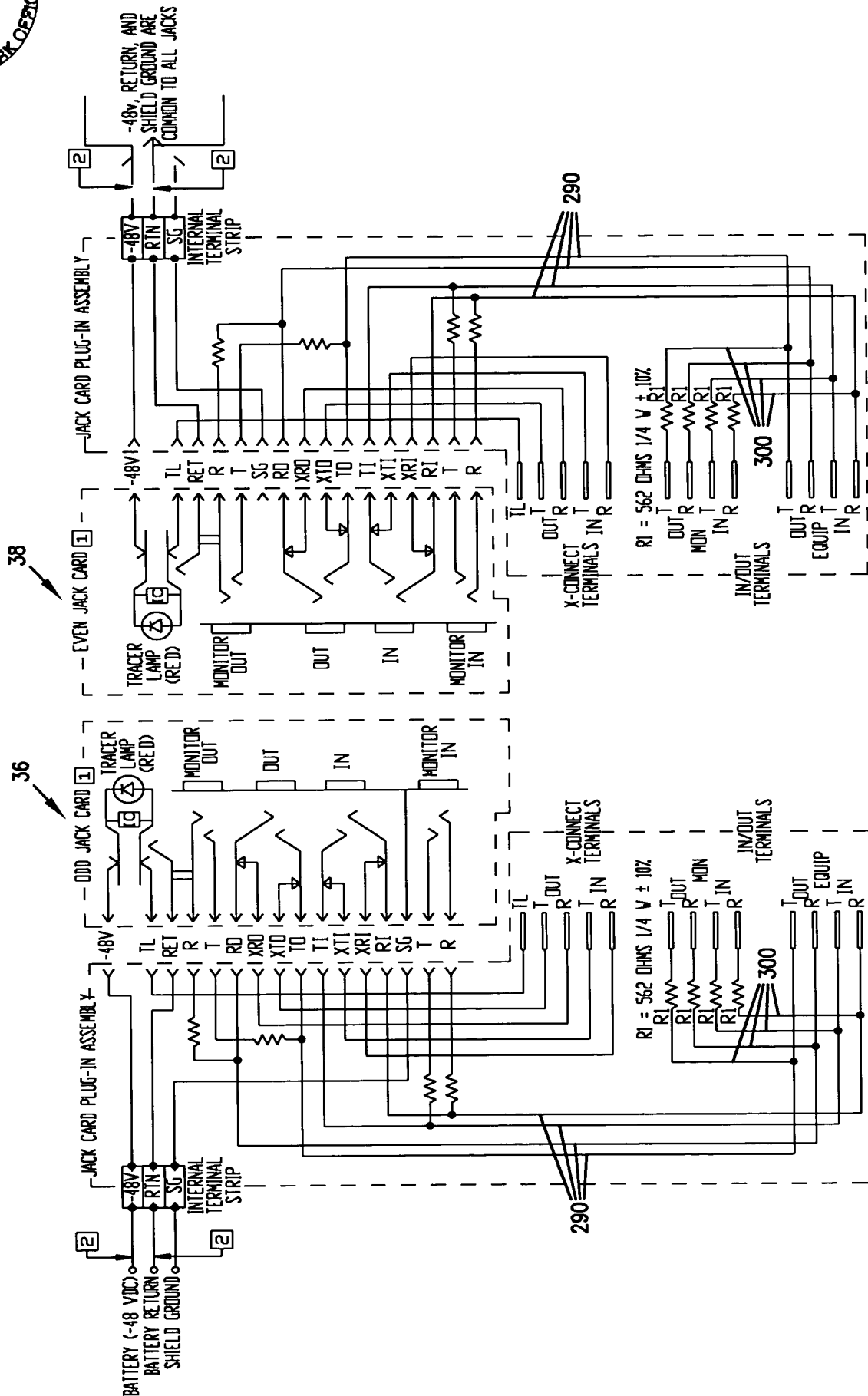


FIG. 9C



**FIG. 10A** CIRCUIT SCHEMATIC  
 ODD JACK POSITION

**FIG. 10B** CIRCUIT SCHEMATIC  
 EVEN JACK POSITION